Reliability evaluation results and plan for

New Molding Compound on I^2PAK, TO-220,TO-247 manufactured in Shenzhen (China) and Bouskoura (Morocco)

Automotive

Process change

General Information	
Commercial Product:	STI47N60DM6AG,STW19NM60N, STW36NM60ND,STW65N65DM2AG, STW75NF30AG,STW78N65M5, STI55NF03L,STP100NF04, STP120N4F6,STP130NS04ZB-MT, STP80NS04ZB STP315N10F7, STP80NF55-08,STP85NF55L-E
Product Line:	PQ6LA1,M264A1,F26LA1,FQF9A1, MM3MA1, M5F9A1, EDDA1, ED4JA1, 6D4FA1,B64JA1,OD0KA1,AD5HA1,E35 HA1,4D4FA1,B587A1
Product Description:	Power MOSFET, Power BIPOLAR
Package:	I^2PAK, TO-220, TO-247
Silicon Technology:	MDmesh™ DM6, MDmesh™ II, FDmesh™ II,MDmesh™ DM2 STripFET™ II,MDmesh™ M5, STripFET™ F6,MESH OVERLAY™ STripFET™ F7,STripFET™ F3, Power BIPOLAR
Division:	Power Transistor Macro-Division

Traceability	
Diffusion Plant:	SG6" - SG8" (Singapore) CT6" - CT8" Catania (Italy)
Assembly Plant:	STS Shenzhen (China) Bouskoura (Morocco)
Reliability Lab:	Catania (Italy)
Passed	☒

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REVISION HISTORY

Version	Date	Author	Changes description
1.0	13 August 2019	A.SETTINIERI	PRELIMINARY REPORT

APPROVED BY:

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1. RELIABILITY EVALUATION OVERVIEW

1.1 Objective

Reliability evaluation for New Molding Compound on I²PAK, TO-220, TO-247 manufactured in Shenzhen (China) and Bouskoura (Morocco)

1.2 Reliability Test Plan

Reliability tests performed on this device are in agreement with ZVEI Guidelines and are listed in the Test Plan. For details on test conditions, generic data used and spec reference see test results summary at Par.3 .

#	Stress	Abrv	Reference	Data type	Test flag	Comments
1	Pre and Post-Stress Electrical Test	TEST	User specification or supplier's standard Specification	1	Y	
2	External Visual	EV	JESD22B-101	1	Y	
3	Parametric Verification	PV	User specification	1	Y	
4	High Temperature Reverse Bias	HTRB	MIL-STD-750-1 M1038 Method A	1	Y	
5	High Temperature Gate Bias	HTGB	JESD 22A-108	1	Y	
6	Pre-conditioning	PC	JESD22A-113	1	Y	
7	Temperature Cycling	TC	JESD22A-104	1	Y	
7a	Temperature Cycling Hot Test	TCHT	JESD22A-104	1	Y	
7a alt	TC Delamination Test	TCDT	JESD22A-104	1	Y	
8	Autoclave	AC	JESD22A-102	1	Y	
9	High Humidity High Temperature Reverse Bias	H3TRB	JESD22A-101	1	Y	
10	Intermittent Operational Life / Thermal Fatigue	IOL / TF	MIL-STD-750 Method 1037	1	Y	
11	ESD Characterization	ESD (HBM,CDM)	AEC Q101-001 and 005	1	Y	
12	Destructive Physical Analysis	DPA	AEC-Q101-004 Section 4	1	Y	
13	Thermal Resistance	TR	JESD24-3, 24-4, 24-6 as appropriate	3	Y	
14	Wire Bond Strength	WBS	MIL-STD-750 Method 2037	3	Y	
15	Bond Shear	BS	AEC-Q101-003	3	Y	
16	Die Shear	DS	MIL-STD-750 Method 2017	3	Y	
17	Dielectric Integrity	DI	AEC-Q101-004 section 3	3	Y	

1.3 Conclusion

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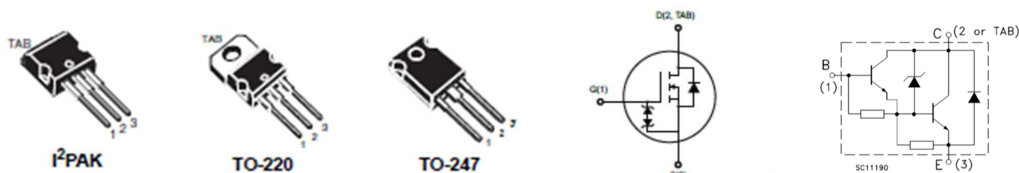
2. DEVICE/TEST VEHICLE CHARACTERISTICS

2.1 Generalities

MDmesh™ DM6, MDmesh™ II,FDmesh™ II,MDmesh™ DM2,STripFET™ II,MDmesh™ M5, STripFET™ F6,MESH OVERLAY™,STripFET™ F7,STripFET™ F3, Power BIPOLAR

2.2 Pin Connection



2.3 Traceability

Reference “Product Baseline” document if existing, else provide following chapters/information:

D.U.T.: STI47N60DM6AG **PACKAGE: I²PAK**

Wafer fab information	
Wafer fab manufacturing location	SG6” (Singapore)
Wafer diameter (inches)	6”
Silicon process technology	MDmesh™ DM6
Die finishing front side (passivation)	TEOS + SiN (Nitride)
Die finishing back side	Ti/Ni/Ag
Die area (Stepping die size)	6850 x 5080 μm^2
Metal levels/Materials	1 / AlCu

Assembly Information	
Assembly plant location	STS Shenzhen (China)
Package code description	I²PAK
Lead frame/Substrate	FRAME TO220 Mon Ve5 OpD/M/Q SelNi/NiP
Die attach material	Preform Pb/Ag/Sn
Wires bonding materials/diameters	Gate Al/Mq 5mils- Source: Al 15mils
Molding compound	Halogen free

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D.U.T.: STW19NM60N PACKAGE: TO-247

Wafer fab information	
Wafer fab manufacturing location	SG8" (Singapore)
Wafer diameter (inches)	8"
Silicon process technology	MDmesh™ II
Die finishing front side (passivation)	SiN (Nitride)
Die finishing back side	Ti/Ni/Ag
Die area (Stepping die size)	4400 x 3200 μm^2
Metal levels/Materials	1 / AlSi

Assembly Information	
Assembly plant location	STS Shenzhen (China)
Package code description	TO-247
Lead frame/Substrate	FRAME TO247 3L Mon Ve6 OpA/Q SelNi/NiP
Die attach material	Preform Pb/Ag/Sn
Wires bonding materials/diameters	Gate Al/Mg 5mils- Source: Al 10mils
Molding compound	Halogen free

D.U.T.: STW36NM60ND PACKAGE: TO-247

Wafer fab information	
Wafer fab manufacturing location	SG6" (Singapore)
Wafer diameter (inches)	6"
Silicon process technology	FDmesh™ II
Die finishing front side (passivation)	SiN (Nitride)
Die finishing back side	Ti/Ni/Ag
Die area (Stepping die size)	6840 x 5050 μm^2
Metal levels/Materials	1 / AlSi

Assembly Information	
Assembly plant location	STS Shenzhen (China)
Package code description	TO-247
Lead frame/Substrate	FRAME TO247 3L Mon Ve6 OpA/Q SelNi/NiP
Die attach material	Preform Pb/Ag/Sn
Wires bonding materials/diameters	Gate Al/Mg 5mils- Source: RIBBON Al 40x6 mils
Molding compound	Halogen free

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D.U.T.: STW65N65DM2AG PACKAGE: TO-247

Wafer fab information	
Wafer fab manufacturing location	SG6” (Singapore)
Wafer diameter (inches)	6”
Silicon process technology	MDmesh™ DM2
Die finishing front side (passivation)	TEOS + SiN (Nitride)
Die finishing back side	Ti/Ni/Ag
Die area (Stepping die size)	10390 x 6850 μm^2
Metal levels/Materials	1 / AlSi

Assembly Information	
Assembly plant location	STS Shenzhen (China)
Package code description	TO-247
Lead frame/Substrate	FRAME TO247 3L Mon Ve6 OpA/Q SelNi/NiP
Die attach material	Preform Pb/Ag/Sn
Wires bonding materials/diameters	Gate Al/Mg 5mils- Source: Al 10mils
Molding compound	Halogen free

D.U.T.: STW75NF30AG PACKAGE: TO-247

Wafer fab information	
Wafer fab manufacturing location	SG6” (Singapore)
Wafer diameter (inches)	6”
Silicon process technology	STripFET™ II
Die finishing front side (passivation)	SiN (Nitride)
Die finishing back side	Ti/Ni/Au
Die area (Stepping die size)	9520 x 6760 μm^2
Metal levels/Materials	1 / AlSi

Assembly Information	
Assembly plant location	STS Shenzhen (China)
Package code description	TO-247
Lead frame/Substrate	FRAME TO247 3L Mon Ve6 OpA/Q SelNi/NiP
Die attach material	Preform Pb/Ag/Sn
Wires bonding materials/diameters	Gate Al 7mils- Source: RIBBON Al 60x8mils
Molding compound	Halogen free

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D.U.T.: STW78N65M5 PACKAGE: TO-247

Wafer fab information	
Wafer fab manufacturing location	CT8" (Catania)
Wafer diameter (inches)	8"
Silicon process technology	MDmesh M5
Die finishing front side (passivation)	SiN (Nitride)
Die finishing back side	Ti/Ni/Ag
Die area (Stepping die size)	10410 x 6810 μm^2
Metal levels/Materials	1 / AlSi

Assembly Information	
Assembly plant location	STS Shenzhen (China)
Package code description	TO-247
Lead frame/Substrate	FRAME TO247 3L Mon Ve6 OpA/Q SelNi/NiP
Die attach material	Preform Pb/Ag/Sn
Wires bonding materials/diameters	Gate Al/Mg 5mils- Source: RIBBON Al 60x8mils
Molding compound	Halogen free

D.U.T.: STI55NF03L PACKAGE: I^2PAK

Wafer fab information	
Wafer fab manufacturing location	CT6" (Catania)
Wafer diameter (inches)	6"
Silicon process technology	STripFET™ II
Die finishing front side (passivation)	No Passivation
Die finishing back side	Ti/NiV/Ag
Die area (Stepping die size)	2080 x 2510 μm^2
Metal levels/Materials	1 / AlSi

Assembly Information	
Assembly plant location	STS Shenzhen (China)
Package code description	I^2PAK
Lead frame/Substrate	FRAME TO220 Mon Ve5 OpD/H/Q SelNi/NiP
Die attach material	Preform Pb/Ag/Sn
Wires bonding materials/diameters	Gate Al/Mg 5mils- Source: Al 15mils
Molding compound	Halogen free

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D.U.T.: STP100NF04 PACKAGE: TO-220

Wafer fab information	
Wafer fab manufacturing location	SG6" (Singapore)
Wafer diameter (inches)	6"
Silicon process technology	STripFET™ II
Die finishing front side (passivation)	Al
Die finishing back side	Ti/Ni/Au
Die area (Stepping die size)	4630 x 5660 μm^2
Metal levels/Materials	1 / AlSi

Assembly Information	
Assembly plant location	STS Shenzhen (China)
Package code description	TO-220
Lead frame/Substrate	FRAME TO220 Mon Ve1 OpD/H/L 20u PINi/NiP
Die attach material	Preform Pb/Ag/Sn
Wires bonding materials/diameters	Gate Al/Mg 5mils- Source: Al 15mils
Molding compound	Halogen free

D.U.T.: STP315N10F7 PACKAGE: TO-220

Wafer fab information

Wafer fab information	
Wafer fab manufacturing location	CT8" (Catania)
Wafer diameter (inches)	8"
Silicon process technology	STripFET™ F7
Die finishing front side (passivation)	TEOS + SiN (Nitride)
Die finishing back side	Ti/NiV/Ag
Die area (Stepping die size)	6340 x 4600 μm^2
Metal levels/Materials	1 / AlCu

Assembly information

Assembly Information	
Assembly plant location	STS Shenzhen (China)
Package code description	TO-220
Leadframe/Substrate	FRAME TO220 Mon Ve1 OpD/M PINi/NiP
Die attach material	PREFORM Pb/Ag/Sn
Wires bonding materials/diameters	Gate Al/Mg 5mils- Source: Al 20mils
Molding compound	Halogen free

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D.U.T.: STP120N4F6 PACKAGE: TO-220

Wafer fab information

Wafer fab information	
Wafer fab manufacturing location	CT8" (Catania)
Wafer diameter (inches)	8"
Silicon process technology	STripFET™ F6
Die finishing front side (passivation)	TEOS + SiN (Nitride)
Die finishing back side	Ti/NiV/Au
Die area (Stepping die size)	2640 x 3860 μm^2
Metal levels/Materials	1 / AlCu

Assembly information

Assembly Information	
Assembly plant location	Bouskoura (Morocco)
Package code description	TO-220
Leadframe/Substrate	FRAME TO220 Mon Ve1 OpD/H/L 20u PlNi/NiP
Die attach material	PREFORM Pb/Ag/Sn
Wires bonding materials/diameters	Gate Al/Mg 5mils- Source: Al 15mils
Molding compound	Halogen free

D.U.T.: STP130NS04ZB-MT PACKAGE: TO-220

Wafer fab information

Wafer fab information	
Wafer fab manufacturing location	CT6" (Catania)
Wafer diameter (inches)	6"
Silicon process technology	MESH OVERLAY™
Die finishing front side (passivation)	SiN (Nitride)
Die finishing back side	Ti/Ni/Au
Die area (Stepping die size)	5680 x 3860 μm^2
Metal levels/Materials	AlSi

Assembly information

Assembly Information	
Assembly plant location	Bouskoura (Morocco)
Package code description	TO-220
Leadframe/Substrate	FRAME TO220 Mon Ve4 OpD/M/N SelNi/NiP
Die attach material	PREFORM Pb/Ag/Sn
Wires bonding materials/diameters	Gate Al/Mg 5mils- Source: Al 15mils
Molding compound	Halogen free

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D.U.T.: STP80NS04ZB PACKAGE: TO-220

Wafer fab information

Wafer fab information	
Wafer fab manufacturing location	CT6” (Catania)
Wafer diameter (inches)	6”
Silicon process technology	MESH OVERLAY™
Die finishing front side (passivation)	SiN (Nitride)
Die finishing back side	Ti/Ni/Au
Die area (Stepping die size)	5680 x 3860 μm^2
Metal levels/Materials	AlSi

Assembly information

Assembly Information	
Assembly plant location	Bouskoura (Morocco)
Package code description	TO-220
Leadframe/Substrate	FRAME TO220 Mon Ve4 OpD/M/N SelNi/NiP
Die attach material	PREFORM Pb/Ag/Sn
Wires bonding materials/diameters	Gate Al/Mg 5mils- Source: Al 15mils
Molding compound	Halogen free

D.U.T.: STP80NF55-08 PACKAGE: TO-220

Wafer fab information

Wafer fab information	
Wafer fab manufacturing location	SG6” (Singapore)
Wafer diameter (inches)	6”
Silicon process technology	STripFET™ II
Die finishing front side (passivation)	NO PASSIVATION
Die finishing back side	Ti/Ni/Au
Die area (Stepping die size)	4100 x 5050 μm^2
Metal levels/Materials	AlSi

Assembly information

Assembly Information	
Assembly plant location	Bouskoura (Morocco)
Package code description	TO-220
Leadframe/Substrate	FRAME TO220 Mon Ver 1 Opt D/H/L/N SelNi/NiP
Die attach material	PREFORM Pb/Ag/Sn
Wires bonding materials/diameters	Gate Al/Mg 5mils- Source: Al 15mils
Molding compound	Halogen free

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D.U.T.: STP85NF55L-E PACKAGE: TO-220

Wafer fab information

Wafer fab information	
Wafer fab manufacturing location	SG6” (Singapore)
Wafer diameter (inches)	6”
Silicon process technology	STripFET™ II
Die finishing front side (passivation)	SiN (Nitride)
Die finishing back side	Ti/Ni/Ag
Die area (Stepping die size)	4460 x 5050 μm^2
Metal levels/Materials	AlSi

Assembly information

Assembly Information	
Assembly plant location	Bouskoura (Morocco)
Package code description	TO-220
Leadframe/Substrate	FRAME TO220 Mon Ve4 OpD/M/N SelNi/NiP
Die attach material	PREFORM Pb/Ag/Sn
Wires bonding materials/diameters	Gate Al/Mg 5mils- Source: Al 15mils
Molding compound	Halogen free

D.U.T.: STP95N4F3 PACKAGE: TO-220

Wafer fab information

Wafer fab information	
Wafer fab manufacturing location	CT8” Catania (Italy)
Wafer diameter (inches)	8”
Silicon process technology	STripFET™ F3
Die finishing front side (passivation)	TEOS+ SiN (Nitride)
Die finishing back side	Ti/Ni/Ag
Die area (Stepping die size)	3550 x 2890 μm^2
Metal levels/Materials	1 / AlCu

Assembly information

Assembly Information	
Assembly plant location	Bouskoura (Morocco)
Package code description	TO-220
Leadframe/Substrate	FRAME TO220 Mon Ver 1 Opt D/H/L/N SelNi/NiP
Die attach material	PREFORM Pb/Ag/Sn
Wires bonding materials/diameters	Gate Al/Mg 5mils- Source: Al 15mils
Molding compound	Halogen free

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D.U.T.: BU941ZT PACKAGE: TO-220

Wafer fab information	
Wafer fab manufacturing location	SG6" (Singapore)
Wafer diameter (inches)	6"
Silicon process technology	Power BIPOLAR
Die finishing front side (passivation)	PSG
Die finishing back side	Ti/Ni/Ag
Die area (Stepping die size)	4560 x 5560 μm^2
Metal levels/Materials	Al

Assembly Information	
Assembly plant location	STS Shenzhen (China)
Package code description	TO-220
Lead frame/Substrate	FRAME TO220 Mon Ver 1 Opt D/H 20u PlNi/NiP
Die attach material	PREFORM Pb/Ag/Sn
Wires bonding materials/diameters	Gate Al/Mg 7mils- Source: Al 15mils
Molding compound	Halogen free

Reliability Testing Information	
Reliability laboratory location	Catania (Italy)
Electrical testing location	Catania (Italy)

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3. TESTS RESULTS SUMMARY

3.1 Lot Information

<table>
<tr><th colspan="7">High Voltage Test Vehicles</th></tr>
<tr><th>Lot #</th><th>Commercial Product</th><th>Silicon line</th><th>Package</th><th>Technology</th><th>Assembly plant</th><th>Note</th></tr>
<tr><td>1</td><td rowspan="3">STI47N60DM6AG</td><td rowspan="3">PQ6L</td><td rowspan="3">I²PAK</td><td rowspan="3">MDmesh™ DM6</td><td rowspan="3">SHENZHEN B/E</td><td></td></tr>
<tr><td>2</td><td></td></tr>
<tr><td>3</td><td></td></tr>
<tr><td>4</td><td>STW19NM60N</td><td>M264</td><td>TO-247</td><td>MDmesh™ II</td><td>SHENZHEN B/E</td><td></td></tr>
<tr><td>5</td><td>STW36NM60ND</td><td>F26L</td><td>TO-247</td><td>FDmesh™ II</td><td>SHENZHEN B/E</td><td></td></tr>
<tr><td>6</td><td>STW65N65DM2AG</td><td>FQF9</td><td>TO-247</td><td>MDmesh™ DM2</td><td>SHENZHEN B/E</td><td></td></tr>
<tr><td>7</td><td>STW75NF30AG</td><td>MM3M</td><td>TO-247</td><td>STripFET™ II</td><td>SHENZHEN B/E</td><td></td></tr>
<tr><td>8</td><td>STW78N65M5</td><td>M5F9</td><td>TO-247</td><td>MDmesh™ M5</td><td>SHENZHEN B/E</td><td></td></tr>
<tr><th colspan="7">Low Voltage Test Vehicles</th></tr>
<tr><td>1</td><td>STI55NF03L</td><td>E33D</td><td>I²PAK</td><td>STripFET™ II</td><td>SHENZHEN B/E</td><td></td></tr>
<tr><td>2</td><td rowspan="3">STP100NF04</td><td rowspan="3">ED4J</td><td rowspan="3">TO-220</td><td rowspan="3">STripFET™ II</td><td rowspan="3">SHENZHEN B/E</td><td></td></tr>
<tr><td>3</td><td></td></tr>
<tr><td>4</td><td></td></tr>
<tr><td>5</td><td>STP120N4F6</td><td>6D4F</td><td>TO-220</td><td>STripFET™ F6</td><td>BOUSKOURA B/E</td><td></td></tr>
<tr><td>6</td><td>STP130NS04ZB-MT</td><td>B64J</td><td>TO-220</td><td>MESH OVERLAY™</td><td>BOUSKOURA B/E</td><td></td></tr>
<tr><td>7</td><td rowspan="3">STP80NS04ZB</td><td rowspan="3">B64J</td><td rowspan="3">TO-220</td><td rowspan="3">MESH OVERLAY™</td><td rowspan="3">BOUSKOURA B/E</td><td rowspan="3"></td></tr>
<tr><td>8</td></tr>
<tr><td>9</td></tr>
<tr><td>10</td><td rowspan="3">STP315N10F7</td><td rowspan="3">OD0K</td><td rowspan="3">TO-220</td><td rowspan="3">STripFET™ F7</td><td rowspan="3">SHENZHEN B/E</td><td></td></tr>
<tr><td>11</td><td></td></tr>
<tr><td>12</td><td></td></tr>
<tr><td>13</td><td>STP80NF55-08</td><td>AD5H</td><td>TO-220</td><td>STripFET™ II</td><td>BOUSKOURA B/E</td><td></td></tr>
<tr><td>14</td><td>STP85NF55L-E</td><td>E35H</td><td>TO-220</td><td>STripFET™ II</td><td>BOUSKOURA B/E</td><td></td></tr>
<tr><th colspan="7">Power BIPOLAR Test Vehicles</th></tr>
<tr><td>1</td><td>BU941ZT</td><td>B587</td><td>TO-220</td><td>Power BIPOLAR</td><td>SHENZHEN B/E</td><td></td></tr>
</table>

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3.2 Test results summary

High Voltage results:

Test	Std ref.	Conditions	SS	Steps	Failure/SS							
					Lot 1	Lot 2	Lot 3	Lot 4	Lot 5	Lot 6	Lot 7	Lot 8
TEST	User specification	All qualification parts tested per the requirements of the appropriate device specification.			462	77	77	231	462	462	462	462
External visual	JESD22 B-101	All devices submitted for testing			462	77	77	231	462	462	462	462
Silicon oriented Tests												
HTRB	JESD22 A-108	Tj = 150°C, BIAS = 600V	231	168 h	0/77			0/77	0/77			
				500 h	0/77	-	-	0/77	0/77	-	-	-
				1000 h	0/77			0/77	0/77			
		Tj = 150°C, BIAS = 520V	154	168 h						0/77		0/77
				500 h	-	-		-	-	0/77	-	0/77
				1000 h						0/77		0/77
		Tj = 150°C, BIAS = 300V	77	168 h							0/77	
				500 h	-	-	-	-	-	-	0/77	-
				1000 h							0/77	
HTGB	JESD22 A-108	Tj = 150°C, BIAS = 25V	231	168 h						0/77	0/77	0/77
				500 h	-	-	-	-	-	0/77	0/77	0/77
				1000 h						0/77	0/77	0/77
		Tj = 150°C, BIAS = 20V	154	168 h	0/77				0/77			
				500 h	0/77	-	-	-	0/77	-	--	
				1000 h	0/77				0/77			
Package oriented Tests												
TC	JESD22 A-104	TA=-55°C TO 150°C	616	100cy	0/77	0/77	0/77	0/77	0/77	0/77	0/77	0/77
				500cy	0/77	0/77	0/77	0/77	0/77	0/77	0/77	0/77
				1000cy								
TCHT	JESD22 A-104 Appendix 6	125°C TEST after TC	616									
		decap and wire pull for parts with internal bond wire sizes 5 mil diameter and less	40									
TCDT		100% C-SAM inspection after TC	616									
AC	JESD22 A-102	TA=121°C ; PA=2ATM	308	96h	0/77	-	-	-	0/77	0/77	0/77	0/77
H3TRB	JESD22 A-101	TA=85°C ; RH=85% BIAS= 100V	385	168 h	0/77	-	-	0/77	0/77	0/77	0/77	0/77
				500 h	0/77	-	-	0/77	0/77	0/77	0/77	0/77
				1000 h	0/77	-	-	0/77	0/77	0/77	0/77	0/77
IOL	MIL-STD-750 Method 1037	ΔTj ≥100°C	308	15Kcy	0/77	-	-	-	0/77	0/77	0/77	0/77
ESD	AEC Q101-001,002 and 005	CDM / HBM	480									
D.P.A.	AEC-Q101-004 Section 4	Devices after H3TRB - TC	32									
Thermal Resistance	JESD24-3, 24-4, 24-6 as appropriate		10 each Pre-post change									
Wire Bond Strength	MIL-STD-750 Method 2037		10 bonds from min of 5 devices									
Bond Shear	AEC-Q101-003		10 bonds from min of 5 devices									
Die Shear	MIL-STD-750 Method 2017		10									
Dielectric Integrity	AEC-Q101-004 section 3		10									

Final results available for HV products	Lot 1	Lot 2	Lot 3	Lot 4	Lot 5	Lot 6	Lot 7	Lot 8
	WK44							

This report and its contents shall not be disclosed to a third party, except in full, without previous written agreement by STMicroelectronics

Low Voltage results:

Test	Std ref.	Conditions	SS	Steps	Failure/SS								
					Lot 1	Lot 2	Lot 3	Lot 4	Lot 5	Lot 6	Lot 7	Lot 8	Lot 9
TEST	User specification	All qualification parts tested per the requirements of the appropriate device specification.			77	462	462	462	462	462	462	462	462
External visual	JESD22 B-101	All devices submitted for testing			77	462	462	462	462	462	462	462	462
Silicon oriented Tests													
HTRB	JESD22 A-108	Tj = 175°C, BIAS = 30V	-	-	-	-	-	-	-	-	-	-	-
		Tj = 175°C, BIAS = 40V	616	168 h		0/77	0/77	0/77	0/77	0/77			
				500 h		0/77	0/77	0/77	0/77	0/77			
				1000 h		0/77	0/77	0/77					
		Tj = 175°C, BIAS = 55V	-	-	-	-	-	-	-	-	-	-	-
		Tj = 175°C, BIAS = 100V	-	-	-	-	-	-	-	-	-	-	-
HTGB	JESD22 A-108	Tj = 175°C, BIAS = 15V	539	168 h	-	0/77	0/77	0/77		0/77			
				500 h	-	0/77	0/77	0/77		0/77			
				1000 h	-	0/77	0/77	0/77					
		Tj = 175°C, BIAS = 20V	77	168 h	-				0/77				
				500 h	-				0/77				
				1000 h	-								
TC	JESD22 A-104	TA=-55°C TO 150°C	693	100cy	0/77	0/77	0/77	0/77	0/77	0/77	0/77	0/77	0/77
				500cy	0/77	0/77	0/77	0/77	0/77	0/77	0/77	0/77	0/77
				1000cy									
TCHT	JESD22 A-104 Appendix 6	125°C TEST after TC	693										
		decap and wire pull for parts with internal bond wire sizes 5 mil diameter and less	45										
TCDT		100% C-SAM inspection after TC	693										
AC	JESD22 A-102	TA=121°C ; PA=2ATM	616	96h		0/77	0/77	0/77					
H3TRB	JESD22 A-101	TA=85°C ; RH=85% BIAS= 32V	385	168 h		0/77	0/77	0/77	0/77	0/77			
				500 h		0/77	0/77	0/77	0/77	0/77			
				1000 h		0/77	0/77	0/77					
		TA=85°C ; RH=85% BIAS= 80V	-	-	-	-	-	-	-	-	-	-	-
		TA=85°C ; RH=85% BIAS= 44V	-	-	-	-	-	-	-	-	-	-	-
IOL	MIL-STD-750 Method 1037	ΔTj ≥100°C		15Kcy		0/77	0/77	0/77					
ESD	AEC Q101-001,002 and 005	CDM / HBM	300										
D.P.A.	AEC-Q101-004 Section 4	Devices after H3TRB - TC	36										
Thermal Resistance	JESD24-3, 24-4, 24-6 as appropriate		10 each Pre-post change										
Wire Bond Strength	MIL-STD-750 Method 2037		10 bonds from min of 5 devices										
Bond Shear	AEC-Q101-003		10 bonds from min of 5 devices 5										
Die Shear	MIL-STD-750 Method 2017		10										
Dielectric Integrity	AEC-Q101-004 section 3		10										

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Test	Std ref.	Conditions	SS	Steps	Failure/SS				
					Lot 10	Lot 11	Lot 12	Lot 13	Lot 14
TEST	User specification	All qualification parts tested per the requirements of the appropriate device specification.			462	462	462	462	462
External visual	JESD22 B-101	All devices submitted for testing			462	462	462	462	462
Silicon oriented Tests									
HTRB	JESD22 A-108	Tj = 175°C, BIAS = 30V	-	-	-	-	-	-	-
		Tj = 175°C, BIAS = 40V	-	-	-	-	-	-	-
		Tj = 175°C, BIAS = 55V	154	168 h	-	-	-	0/77	0/77
				500 h				0/77	0/77
				1000 h					
		Tj = 175°C, BIAS = 100V	231	168 h	0/77	0/77	0/77	-	-
				500 h	0/77	0/77	0/77		
				1000 h	0/77	0/77	0/77		
HTGB	JESD22 A-108	Tj = 175°C, BIAS = 15V	154	168 h	-	-	-	0/77	0/77
				500 h				0/77	0/77
				1000 h					
		Tj = 175°C, BIAS = 20V	231	168 h	0/77	0/77	0/77	-	-
				500 h	0/77	0/77	0/77		
				1000 h	0/77	0/77	0/77		
Package oriented Tests									
TC	JESD22 A-104	TA=-55°C TO 150°C	385	100cy	0/77	0/77	0/77	0/77	0/77
				500cy	0/77	0/77	0/77	0/77	0/77
				1000cy					
TCHT	JESD22 A-104 Appendix 6	125°C TEST after TC	385						
		decap and wire pull for parts with internal bond wire sizes 5 mil diameter and less	25						
TCDT		100% C-SAM inspection after TC	385						
AC	JESD22 A-102	TA=121°C ; PA=2ATM	385	96h	0/77	0/77	0/77	Wk35	Wk35
H3TRB	JESD22 A-101	TA=85°C ; RH=85% BIAS= 32V	-	1000 h	-	-	-	-	-
		TA=85°C ; RH=85% BIAS= 80V	231	168 h	0/77	0/77	0/77	-	-
				500 h	0/77	0/77	0/77		
				1000 h					
		TA=85°C ; RH=85% BIAS= 44V	154	168 h	-	-	-	0/77	0/77
				500 h				0/77	0/77
				1000 h					
IOL	MIL-STD-750 Method 1037	ΔTj ≥100°C	385	15Kcy	0/77	0/77	0/77		
ESD	AEC Q101-001,002 and 005	CDM / HBM	300						
D.P.A.	AEC-Q101-004 Section 4	Devices after H3TRB - TC	20						
Thermal Resistance	JESD24-3, 24-4, 24-6 as appropriate		10 each Pre-post change						
Wire Bond Strength	MIL-STD-750 Method 2037		10 bonds from min of 5 devices						
Bond Shear	AEC-Q101-003		10 bonds from min of 5 devices 5						
Die Shear	MIL-STD-750 Method 2017		10						
Dielectric Integrity	AEC-Q101-004 section 3		10						

Final results available for LV products	**Lot 1**	**Lot 2**	**Lot 3**	**Lot 4**	**Lot 5**	**Lot 6**	**Lot 7**	**Lot 8**	**Lot 9**	**Lot 10**	**Lot 11**	**Lot 12**	**Lot 13**	**Lot 14**
	WK44	WK48			WK45	WK45	WK47			WK 48			WK45	WK45

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Power BIPOLAR results:

Test	Std ref.	Conditions	SS	Steps	Failure/SS Lot 1
TEST	User specification	All qualification parts tested per the requirements of the appropriate device specification.			385
External visual	JESD22 B-101	All devices submitted for testing			385
Silicon oriented Tests					
HTRB	JESD22 A-108	Tj = 175°C, BIAS = 280V	77	168 h	0/77
				500 h	0/77
				1000 h	0/77
TC	JESD22 A-104	TA=-55°C TO 150°C	77	100cy	0/77
				500cy	0/77
				1000cy	
TCHT	JESD22 A-104 Appendix 6	125°C TEST after TC	77		
		decap and wire pull for parts with internal bond wire sizes 5 mil diameter and less	5		
TCDT		100% C-SAM inspection after TC	77		
AC	JESD22 A-102	TA=121°C ; PA=2ATM	77	96h	0/77
H3TRB	JESD22 A-101	TA=85°C ; RH=85% BIAS= 100V		1000 h	0/77
					0/77
					0/77
IOL	MIL-STD-750 Method 1037	ΔTj ≥100°C		15Kcy	0/77
ESD	AEC Q101-001,002 and 005	CDM / HBM		60	
D.P.A.	AEC-Q101-004 Section 4	Devices after H3TRB - TC		4	
Thermal Resistance	JESD24-3, 24-4, 24-6 as appropriate		10 each Pre-post change		
Wire Bond Strength	MIL-STD-750 Method 2037		10 bonds from min of 5 devices		
Bond Shear	AEC-Q101-003		10 bonds from min of 5 devices 5		
Die Shear	MIL-STD-750 Method 2017		10		
Dielectric Integrity	AEC-Q101-004 section 3		10		

Final results available for Power BIPOLAR product	Lot 1
	WK48

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Catania, August 30 2019

Automotive Discrete Group (ADG)
Power Transistor Macro-Division
LV & Body Smart Power Macro-Division

Process Change Notification

I²PAK, TO-220, TO-247 New Molding Compound
Shenzhen (China) - Bouskoura (Marocco)
AUTOMOTIVE

Dear Customer,

Following Samsung SDI production discontinuation announcement, followed by ST Corporate Advance Notification PCI CRP/19/11478, sent in April 2019, **this document is announcing the new molding compound for all products assembled in I²PAK, TO-220 and TO-247 package**, manufactured in the plant of Shenzhen (China) and Bouskoura (Marocco).

The new molding compound, guarantees the same quality and electrical characteristics as per current production, products is in full compliance with the ST ECOPACK®2 grade (Halogen Free).

The test vehicles involved in the qualification are listed in the following tables:

High Voltage Business Unit				
Technology	**Test Vehicle**	**Package**	**Assy Plant**	**End of Qual.**
MDmesh™ DM6	STI47N60DM6AG	I²PAK	SHENZHEN B/E	Wk 44/19
MDmesh™ II	STW19NM60N	TO-247	SHENZHEN B/E	Wk 44/19
FDmesh™ II	STW36NM60ND	TO-247	SHENZHEN B/E	Wk 44/19
MDmesh™ DM2	STW65N65DM2AG	TO-247	SHENZHEN B/E	Wk 44/19
STripFET™ II	STW75NF30AG	TO-247	SHENZHEN B/E	Wk 44/19
MDmesh™ M5	STW78N65M5	TO-247	SHENZHEN B/E	Wk 44/19

Low Voltage Business Unit				
Technology	**Test Vehicle**	**Package**	**Assy Plant**	**End of Qual.**
STripFET™ II	STI55NF03L	I²PAK	SHENZHEN B/E	Wk 44/19
STripFET™ II	STP100NF04	TO-220	SHENZHEN B/E	Wk 48/19
STripFET™ F6	STP120N4F6	TO-220	BOUSKOURA B/E	Wk 45/19
MESH OVERLAY™	STP130NS04ZB-MT	TO-220	BOUSKOURA B/E	Wk 45/19
STripFET™ F7	STP315N10F7	TO-220	SHENZHEN B/E	Wk 48/19
STripFET™ II	STP80NF55-08	TO-220	BOUSKOURA B/E	Wk 45/19
MESH OVERLAY™	STP80NS04ZB	TO-220	BOUSKOURA B/E	Wk 45/19
STripFET™ II	STP85NF55L-E	TO-220	BOUSKOURA B/E	Wk 45/19
STripFET™ F3	STP95N4F3	TO-220	BOUSKOURA B/E	Wk 45/19

IGBT & IPM Business Unit				
Technology	**Test Vehicle**	**Package**	**Assy Plant**	**End of Qual.**
Power BIPOLAR	BU941ZT	TO-220	SHENZHEN B/E	Wk 48/19

Any other Product related to the above series, even if not expressly included or partially mentioned in the attached table, is affected by this change.

Qualification program and results availability:

The reliability test report plan is provided in attachment to this document.

Samples availability:

Samples of the test vehicle devices will be available on request starting from week 36-2019.
Any other sample request will be processed and scheduled by Power Transistor Division upon request.

Change implementation schedule:

The production start and first shipments will be implemented after week 9 of 2020, after stock depletion.
Delivery of current products will be done until stock depletion of old molding compound.
This is a very special Process Change, the PCN approval has to be as fast as possible. Due to the current market conditions and the large space occupied by the old resin, we are unable to do enough stock.

Marking and traceability:

Unless otherwise stated by customer specific requirement, traceability product assembled in with new molding compound, will be ensured by Q.A. number.

Yours faithfully.